Claims

What is claimed is:

1. A testing circuit for tracking transistor stress degradation comprising:

a first array of P-channel field effect transistors (PFETs) connected in parallel; said first array of PFETs being stressed by applying a low gate input and a high source and a high drain for the PFETs during a stress period; and said first array of PFETs being tested by operating the PFETs in a saturated region during a test period; and

a reference array of PFETs not being stressed during the stress period and said reference array of PFETs being activated for testing to compare a saturated drain current performance with said first array of PFETs during the test period.

2. A testing circuit as recited in claim 1 includes a first current source N-channel FET (NFET) device coupled to said first array of PFETs; and a test signal input applied to a gate of said first current source NFET device to activate said current source NFET device during the test period.

3. A testing circuit as recited in claim 2 includes a second current source N-channel FET (NFET) device coupled to said reference array of PFETs; and said test signal input applied to a gate of said second current source NFET device to activate said current source NFET device for testing; said first and said second NFET devices being substantially identical devices.

4. A testing circuit as recited in claim 3 includes at least one additional NFET device connected in parallel with said second current source NFET device coupled to said reference array of PFETs; said at least one additional NFET device for supplying a predetermined amount of additional load current to reference array of PFETs.

5. A testing circuit as recited in claim 4 wherein said at least one additional NFET device having a set width equal to a selected percent of a width of said substantially identical first and said second NFET devices; said set width of said at least one additional NFET device selectively provided to identify a predefined level of degradation of said first array of PFETs.

6. A testing circuit as recited in claim 4 includes a reference NFET device coupled between a respective source of each of said first and said second current source NFET devices and said at least one additional NFET device and ground for level shifting.

7. A testing circuit as recited in claim 4 includes a gated input stage comparator coupled to said first array of PFETs and said reference array of PFETs and receiving said test signal input to activate said gated input stage comparator during the test period.

8. A testing circuit as recited in claim 7 wherein said gated input stage comparator has a first input connected to drain connections of said first array of PFETs and said first current source NFET device for comparison with a second input connected to the drain connections said reference array of PFETs and said second current source NFET device and said at least one additional NFET device.

9. A testing circuit as recited in claim 1 wherein said first array of PFETs is stressed by applying a continuous low gate input to the PFETs during the stress period.

10. A testing circuit as recited in claim 1 wherein said first array of PFETs is stressed by applying a dynamic low gate input to the PFETs having a selected duty cycle during the stress period.

11. A testing circuit as recited in claim 10 wherein said dynamic low gate input to the PFETs having a selected duty cycle during the stress period is provided by an oscillator and combinational logic.

12. A method for tracking transistor stress degradation comprising the steps of:

providing a first array of P-channel field effect transistors (PFETs) connected in parallel;

applying a low gate input and a high source and a high drain for the PFETs to stress said first array of PFETs during a stress period;

operating the PFETs in a saturated region to test said first array of PFETs during a test period;

providing a reference array of PFETs not being stressed during the stress period; and

activating said reference array of PFETs to compare a saturated drain current performance with said first array of PFETs during the test period.

13. A method for tracking transistor stress degradation as recited in claim 12 wherein the step of operating the PFETs in a saturated region to test said first array of PFETs during a test period includes the steps of coupling a first current source N-channel FET (NFET) device to said first array of PFETs; and applying a test signal input to a gate of said first current source NFET device to activate said current source NFET device during the test period.

14. A method for tracking transistor stress degradation as recited in claim 13 wherein the step of activating said reference array of PFETs to compare a saturated drain current performance with said first array of PFETs during the test period includes the steps of coupling a second current source NFET device to said reference array of PFETs; and applying said test signal input to a gate of said second current source NFET device to activate said current source NFET device during the test period.

15. A method for tracking transistor stress degradation as recited in claim 14 includes the steps of coupling at least one additional NFET device to said reference array of PFETs for supplying a predetermined amount of additional load current to reference array of PFETs during the test period.

16. A method for tracking transistor stress degradation as recited in claim 15 includes the steps of coupling a gated input stage comparator coupled to said first array of PFETs and said reference array of PFETs; and applying said test signal to activate said gated input stage comparator during the test period.

17. A method for tracking transistor stress degradation as recited in claim 12 wherein the step of applying a low gate input and a high source and a high drain for the PFETs to stress said first array of PFETs during a stress period includes the steps of applying a continuous low gate input to the PFETs to stress said first array of PFETs during the stress period.

18. A method for tracking transistor stress degradation as recited in claim 12 wherein the step of applying a low gate input and a high source and a high drain for the PFETs to stress said first array of PFETs during a stress period includes the steps of applying a dynamic low gate input to the PFETs having a selected duty cycle to stress said first array of PFETs during the stress period.